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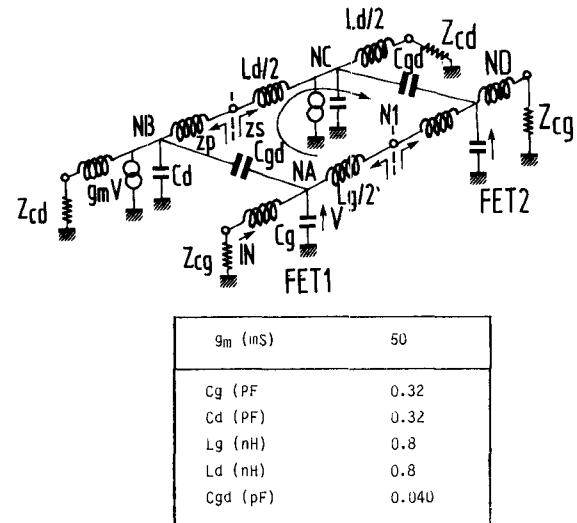


Fig. 1. Basic distributed amplifier with two transistors.

Analysis of the Oscillation Conditions in Distributed Amplifiers

PATRICE GAMAND

Abstract — It has been shown that under certain conditions oscillation phenomena in distributed amplifiers can occur. It has also been demonstrated, using a simplified transistor model and a symmetrical amplifier with lumped circuit elements, that the oscillation depends directly on the transconductance g_m of the active devices. The origin of this oscillation was found to be the "loop" formed in the distributed amplifier structure. The analysis has been experimentally verified in a practical 1-20 GHz monolithic MESFET amplifier. Finally, design guidelines have been established in order to avoid stability problems and to improve the capabilities of high-gain distributed amplifiers.

I. INTRODUCTION

The principle of distributed amplification has been widely applied during the last few years to design multioctave amplifiers. Monolithic [1], [2] as well as hybrid [3], [4] amplifiers have exhibited respectable gain performances over the 2-40 GHz frequency band.

In a simplified approach, the active devices "see" a passive impedance of typically 25Ω , which generally does not lead to instability. Distributed amplifiers therefore have this great advantage with respect to the other solid-state amplifiers. However, under certain conditions, the distributed amplifier can be unstable. The purpose of this paper is to provide some understanding of the oscillation phenomenon in this type of amplifier and to quantitatively examine the factors that determine its magnitude.

II. ANALYSIS OF A BASIC TWO-STAGE DISTRIBUTED AMPLIFIER

Combining several elementary modules, high gain can be achieved over an ultrawide bandwidth. Fig. 1 shows the simplified topology of the amplifier used in the following study and the value used for the analysis.

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The S parameters of such an amplifier, without the gate-to-drain capacitance, have been calculated by Niclas *et al.* [3], but the resulting formulas become extremely complex when the feedback capacitor C_{gd} of the active devices is included and do not make it possible to come to simple conclusions. Consequently, a numerical approach is more appropriate for studying the structure.

The approach is based on a detailed analysis of the impedances Z_p and Z_s , which are, respectively, the impedances of the left-hand and right-hand parts of the circuit seen from any arbitrary reference plane, and on verification of the oscillation condition expressed by

$$\operatorname{Re}(Z_s + Z_p) \leq 0 \quad (1)$$

and

$$\operatorname{Im}(Z_s + Z_p) = 0. \quad (2)$$

This condition can also be expressed in terms of the reflection coefficients Γ_s and Γ_p :

$$|\Gamma_s \Gamma_p| \geq 1 \quad \arg(\Gamma_s \Gamma_p) = 0. \quad (3)$$

When the reference plane is chosen to cut the circuit at nodes N1 (the gate line being cut at N1) and N3 (the drain line being cut at N3), we observe that all impedances are identical (this is due to the symmetry of the structure) and that no oscillation phenomenon can occur when the gate line or the drain line is cut. The same results can be obtained using a nonsymmetrical structure. Therefore, the complete structure with no line cut has to be studied.

A. Global Approach

Curve (a) in Fig. 2 shows the input reflection coefficient of a two-stage structure. We see that, now, in a certain frequency range the magnitude of S_{11} is greater than 1; therefore, instability of the amplifier can occur.

The analysis above shows that the origin of the oscillation can be found in the loop constituted by nodes NA, NB, NC, and ND in Fig. 1. The amplifier oscillates when the gain within the loop becomes too high.

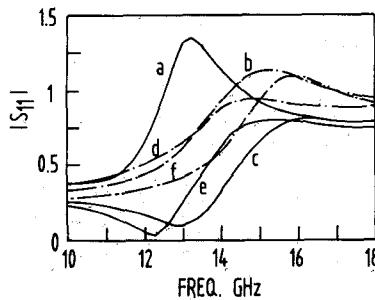


Fig. 2. Input reflection coefficients for six different cases.

B. Analysis of the Loop

In order to determine which elements are causing instability and to understand the oscillation mechanism, certain cases will be analyzed.

The gate-to-drain capacitances C_{gd1} and C_{gd2} will be omitted. In a similar manner, the analysis will be made as a function of the transconductances. (The subscripts 1 and 2 correspond to the first and the second transistor.)

Fig. 2 shows the input reflection coefficient for the following six cases:

- Complete structure of Fig. 1.
- $C_{gd1} = 0$; all other elements are connected.
- $C_{gd2} = 0$; all other elements are connected.
- $g_{m1} = 0$; all other elements are connected.
- $g_{m2} = 0$; all other elements are connected.
- $g_{m2} = 0$ and $C_{gd1} = 0$; all other elements are connected.

From these curves, it can be seen that g_{m1} and C_{gd2} are necessary to generate oscillations.

If either G_{m1} or C_{gd2} is removed, the oscillation phenomenon does not occur. It can also be shown that the transconductance g_{m2} leads to an increase of the oscillations (the gain in the loop is increased) while C_{gd1} has the opposite effect. The amplifier will oscillate if (1) is satisfied.

C. Effect of the Cutoff Frequency of the Transmission Lines and the Size of the Transistors

In the previous section, it has been shown that the magnitude of the input reflection coefficient increases with the transistor transconductance; therefore, the risk of instability also increases. The same effect is obtained with the gate-to-drain capacitance C_{gd0} of the transistor.

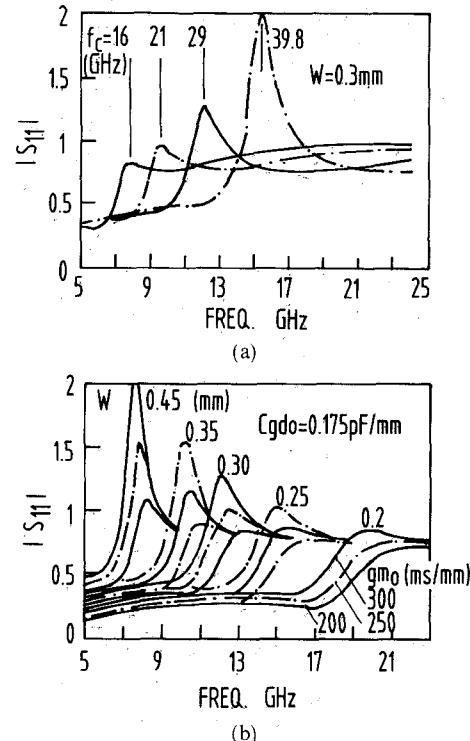
The final basic elements forming the loop are the gate and drain transmission lines, which fix the oscillation frequency. The effect of the characteristics of these lines on the oscillation phenomenon can be studied by considering their characteristic impedance (normally 50Ω) or their cutoff frequency. In this paper only the effect of the cutoff frequency will be considered. To vary the cutoff frequency f_c of the transmission lines, we can change either the gate-to-source capacitance per unit gate width C_{gs0} of the transistors or the size of the transistor. The last case will be considered further.

The gate inductance has been fixed by the low-frequency characteristic impedance:

$$Z_c = \sqrt{\frac{L_{g0}}{C_{gs0}}} = 50 \Omega. \quad (4)$$

TABLE I
ELEMENT VALUES USED IN THE ANALYSIS

Element	Value	Dimension
C_{gd0}	0.175	pF/mm
C_{gs0}	1.1 (varied for f_c)	pF/mm
g_{m0}	varied	mS/mm
R_{ds0}	70	$\Omega \cdot \text{mm}$
R_{i0}	0.4	$\Omega \cdot \text{mm}$

Fig. 3. (a) S_{11} as a function of the cutoff frequency (f_c). (b) S_{11} as a function of frequency for various g_m and f_c .

The cutoff frequency is then equal to

$$f_c = \frac{1}{W * \pi * \sqrt{L_{g0} * C_{gs0}}}. \quad (5)$$

Equations (4) and (5) are given for a T-type LC network, where W is the gate width in millimeters.

In this analysis, the transistor element values were derived from S -parameter measurements of a typical $0.5 \mu\text{m}$ MESFET biased at $I_{ds0}/3$. They are listed in Table I.

Fig. 3(a) shows the input reflection coefficient S_{11} of the structure described in Fig. 1 for different values of the cutoff frequency f_c , taking into account the output conductance $1/R_{ds0}$ and the channel resistance R_{i0} of the active devices in addition to C_{gd0} and g_{m0} . We can see that instability increases with the cutoff frequency of the transmission lines.

The effect of the main elements causing instability has been examined independently. Let us consider now the effect of the size of the transistors. The element values used are listed in Table I. The inductance L_{g0} per unit gate width is calculated according to (4) and (5). The input reflection coefficient S_{11} of the structure

previously used is depicted in Fig. 3(b) for five different gate widths as a function of frequency.

These curves show that the risk of oscillation rapidly increases with the width of the transistors.

D. Discussion

From the analysis carried out above, we can deduce that the oscillations occur at frequency

$$f_0 \frac{1}{\pi * W * \sqrt{2L_{g0}(C_{gs0} + C_{gd0})}} = \frac{f_c}{\sqrt{2\left(1 + \frac{C_{gd}}{C_{gs}}\right)}}. \quad (6)$$

It can also be deduced that, for a given value of W , the risk of oscillation increases with g_m , C_{gd} , and f_c and that the parasitic resistances r_{ds} and R_i tend to moderate the oscillation phenomenon. All the parameters change with the gate width W except the characteristic impedance Z_c . In particular, g_m and C_{gd} increase with W , which tends to increase the risk of oscillation, but f_c decreases correspondingly (see (4)), which has the opposite effect. However, the global effect is an increase with W of the gain on the loop and therefore of the risk of oscillation.

The detailed analysis of a simple structure, including two active devices, has shown that the oscillation phenomenon occurs at high frequency and is due to the internal loop formed by the transconductance and the feedback capacitance of the active devices, combined with the transmission lines. The oscillations cannot be due to reflections at the terminations (Z_{cg} and Z_{cd}) because the oscillation frequency is lower than that of the transmission lines f_c , and an "active" feedback (g_{ml}) is necessary to provide gain in the loop to generate oscillations. It is therefore necessary to analyze the oscillation phenomenon on a more complete structure including the FET parasitic elements to confirm the dependence of the potential instability on the transistor dimensions and to provide more complete design guidelines.

III. DESIGN CONSIDERATIONS

The coupling capacitor C_{gd} of the active devices strongly modifies the behavior of distributed amplifiers, mainly when the frequency is high and transistors with high transconductance are used. In a monolithic design, we attempt to optimize the gate width of the active devices to achieve the required performance. The stability condition for an amplifier is generally defined by the stability factor:

$$K = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|}. \quad (7)$$

If K is >1 , the amplifier is unconditionally stable. If K is <1 , the amplifier is conditionally stable and it oscillates if (1)–(3) are satisfied.

Fig. 4 shows the value of the stability factor as a function of the gate width of a distributed amplifier structure with four transistors. The analysis uses a more complete FET equivalent circuit than in subsection II-C. These parameters are listed in Table II.

It can be seen from the curves of Fig. 4 that increasing the transconductance g_{m0} of the active devices or the gate width leads to instability. These curves also indicate that for a given g_{m0} the gate width is limited to a maximum value to avoid instability problems. Therefore, in the design of distributed amplifiers, the choice of the gate width is important.

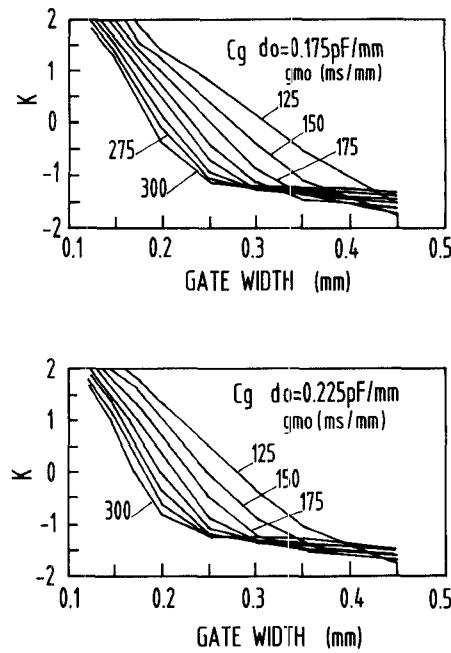


Fig. 4. Stability factor as a function of the gate width of the transistor for various values of g_{m0} and C_{gd0} .

TABLE II
FET EQUIVALENT CIRCUIT USED IN THE ANALYSIS

Element	Value	Dimension
C_{gs0}	1.1	pF/mm
C_{gd0}	0.175	pF/mm
g_{m0}	varied	mS/mm
R_{ds0}	70	$\Omega \cdot \text{mm}$
R_{i0}	0.4	$\Omega \cdot \text{mm}$
R_{s0}	0.6	$\Omega \cdot \text{mm}$
R_{d0}	0.6	$\Omega \cdot \text{mm}$
R_{g0}	12	Ω/mm

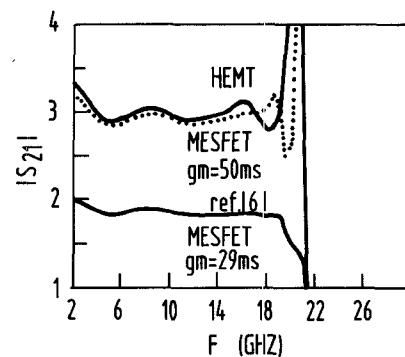


Fig. 5 Simulated gain curves for MESFET amplifiers with $g_m = 29$ mS and $g_m = 50$ mS and for HEMT amplifier using the same circuit design

As an example and also in order to verify the analysis, Fig. 5 presents a simulated gain curve of a 1–20 GHz monolithic GaAs MESFET amplifier [6]. The values of the main elements of the transistor model, C_{gd0} , C_{gs0} , and g_{m0} , are 0.175 pF/mm, 1.1 pF/mm, and 145 mS/mm, respectively.

The inductance per unit gate width of the gate line, L_{g0} , is equal to 2.75 nH/mm (see (4)). The cutoff frequency of the transmission line is $F_c = 28.9$ GHz for a 0.2 mm FET (eq. (5)), and the analysis carried out in Sections II-C and III indicates

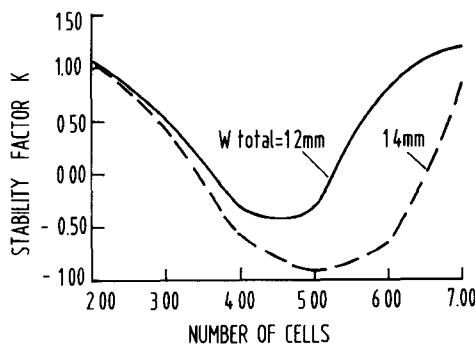


Fig. 6 Effect of the number of cells on amplifiers with the same total gate width.

that the amplifier can be unstable at $F_c = 19$ GHz and when g_{m0} becomes greater than 200 mS/mm (Fig. 5).

If the transconductance g_m changes from 145 mS/mm to 200 mS/mm, the theoretical gain curve in Fig. 5 presents a very high gain around 20 GHz. The stability coefficient K becomes less than unity in this frequency range and the amplifier oscillates at 20.5 GHz. The small difference between this value and the predicted oscillation frequency (F_0) is due to the simplified model used for the analysis.

To improve the gain, another possibility for distributed amplifier design is to increase the number of cells. To improve the frequency bandwidth or the flatness of the gain, the same technique can be used but with smaller transistors.

It is of interest to compare amplifiers with the same total gate width but with a different number of cells.

Fig. 6 presents the minimum stability coefficient K of different amplifiers based on the FET equivalent circuit in Section III (Table II) with $g_{m0} = 250$ mS/mm and at frequency f_0 (eq. (6)). Two total gate widths have been considered. It can be seen that to avoid instability, smaller total gate widths have to be used. However, the lowest value is limited by the decreasing gain-bandwidth product. Fig. 7 also shows that instabilities occur with an increase in the number of cells. This phenomenon is caused by the multiple feedback loops in the amplifier. However, it is considerably diminished when the losses are increased where a large number of cells are used.

IV. DISTRIBUTED AMPLIFIER WITH CASCODE PAIRS

It is well known that using cascode pairs increases the gain of distributed amplifiers. Moreover, the better isolation of this arrangement should attenuate the oscillation phenomenon when the transconductance is increased. This means that the reduction of the coupling between the gate and drain lines makes it possible to avoid oscillations by reducing the gain within the loop.

But another problem occurs in cascode distributed amplifiers. Indeed, the insertion of transmission line lengths between common-source and common-gate FET's is extensively used to increase the gain at high frequency and also to tune the gain response of the amplifier for optimum gain flatness. But these line lengths can generate oscillations and therefore must be carefully chosen as a function of the transconductance of the active devices.

V. CONCLUSION

The occurrence of oscillations in distributed amplifiers has been evaluated. The oscillation mechanism has been elucidated using a simplified transistor model made up of four elements.

The analysis has been extended to amplifiers whose transistors are represented by S -parameter derived models. It has been demonstrated that increasing the transconductance of the transistor can generate oscillations into the loops existing in distributed amplifiers between stages at frequencies around

$$f_0 \frac{1}{\pi * \sqrt{2L(C + C_{gd})}}.$$

This phenomenon occurs when high-transconductance transistors are used (HEMT devices, for example) and it can be reduced using smaller transistors or higher cutoff frequencies.

Improvements in the gain-bandwidth product can be obtained with high transconductances but need lower gate-to-drain feedback capacitances or other structures such as the cascode configuration to reduce the coupling effect between the gate and drain lines.

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Lower Bound on the Eigenvalues of the Characteristic Equation for an Arbitrary Multilayered Gyromagnetic Structure with Perpendicular Magnetization

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Abstract—A layered gyromagnetic waveguiding structure magnetized perpendicularly to interfaces between layers is analyzed. The lower bound on the eigenvalues of the wave equation for this structure is derived using

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